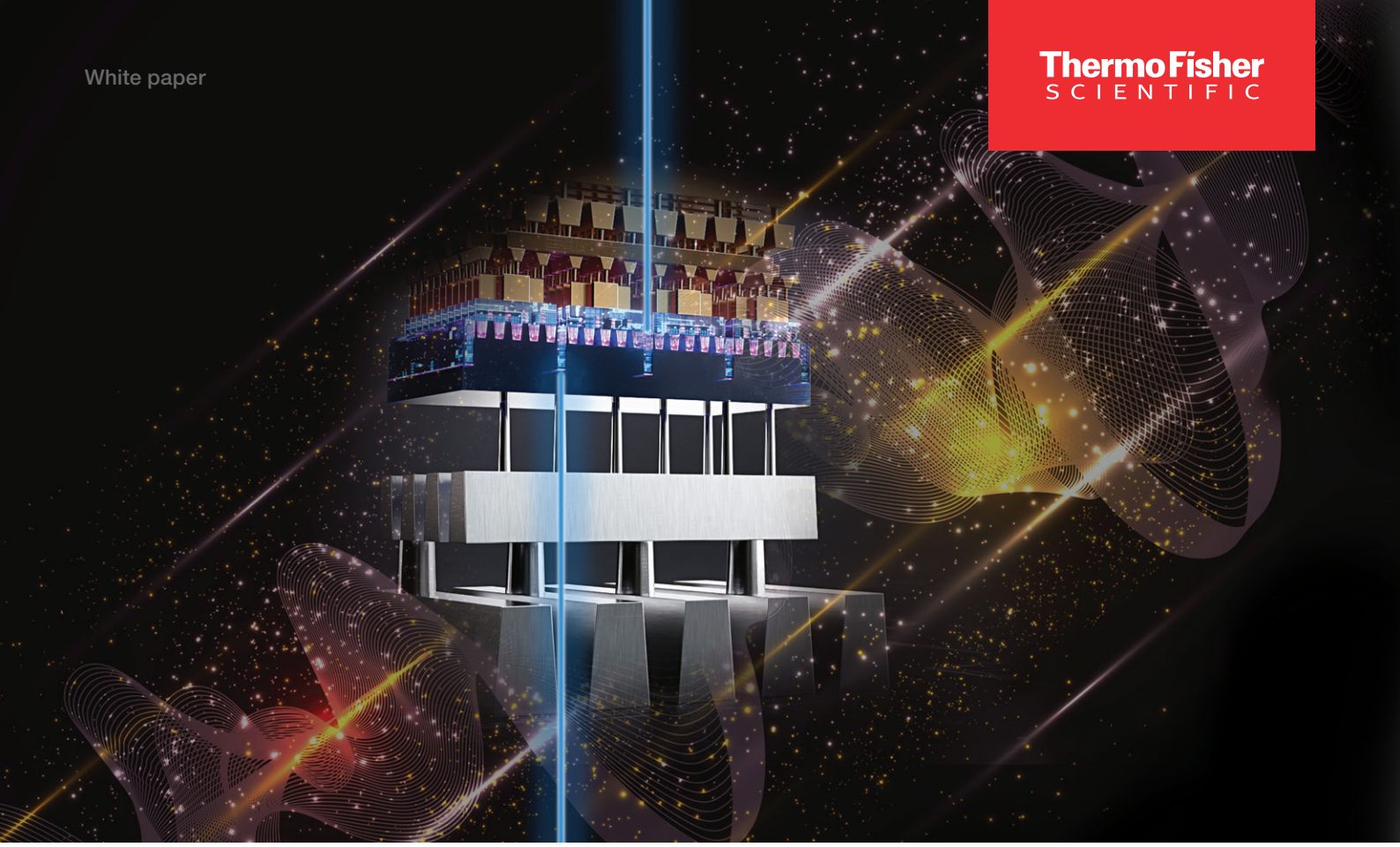
White paper



Failure analysis on advanced logic devices

Multiple inflection points are affecting the entire FA ecosystem

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Keywords

gate-all-around (GAA), advanced logic, nanosheet, yield enhancement, defect analysis, transmission electron microscopy (TEM), TEM sample preparation, delayering, failure analysis, optical probing, ebeam probing, nanoprobing

Summary

The failure analysis (FA) challenges introduced with the latest, most advanced logic technology nodes are significantly greater than anything the industry has seen to date. Advanced logic devices are undergoing significant changes as they move to sub-3 nm technology nodes that include the implementation of gate-all-around (GAA) structures and backside power delivery networks (BPDN). These advancements not only enhance device performance but also impact the traditional FA landscape.

Failure analysis after production electrical testing performs an increasingly essential role at IDMs and foundries. Despite the comprehensive defect inspection and TEM wafer level sample analysis carried out during the manufacturing process, there has been a rise in the detection of defects at the back end of line through electrical testing. While some of these defects may be straightforward and easily identifiable, the reduction in fab process windows and the tightening of device tolerances have led to an increase in subtle, “soft” defects and marginal timing failures. Engineers use failure analysis to identify a failure’s root cause. Advanced logic structures that utilize FinFET or gate-all-around (GAA) structures need precision imaging and elemental data at the atomic scale to fully comprehend the interdependencies between fab process variability and actual device performance. These failures may also be seen at end users, such as the fabless companies and design houses that depend on the performance and quality of these finished devices. To get the performance and reliability they need in their finished product, designers must perform rapid, high-quality root cause analysis to correct issues at their foundry supplier.

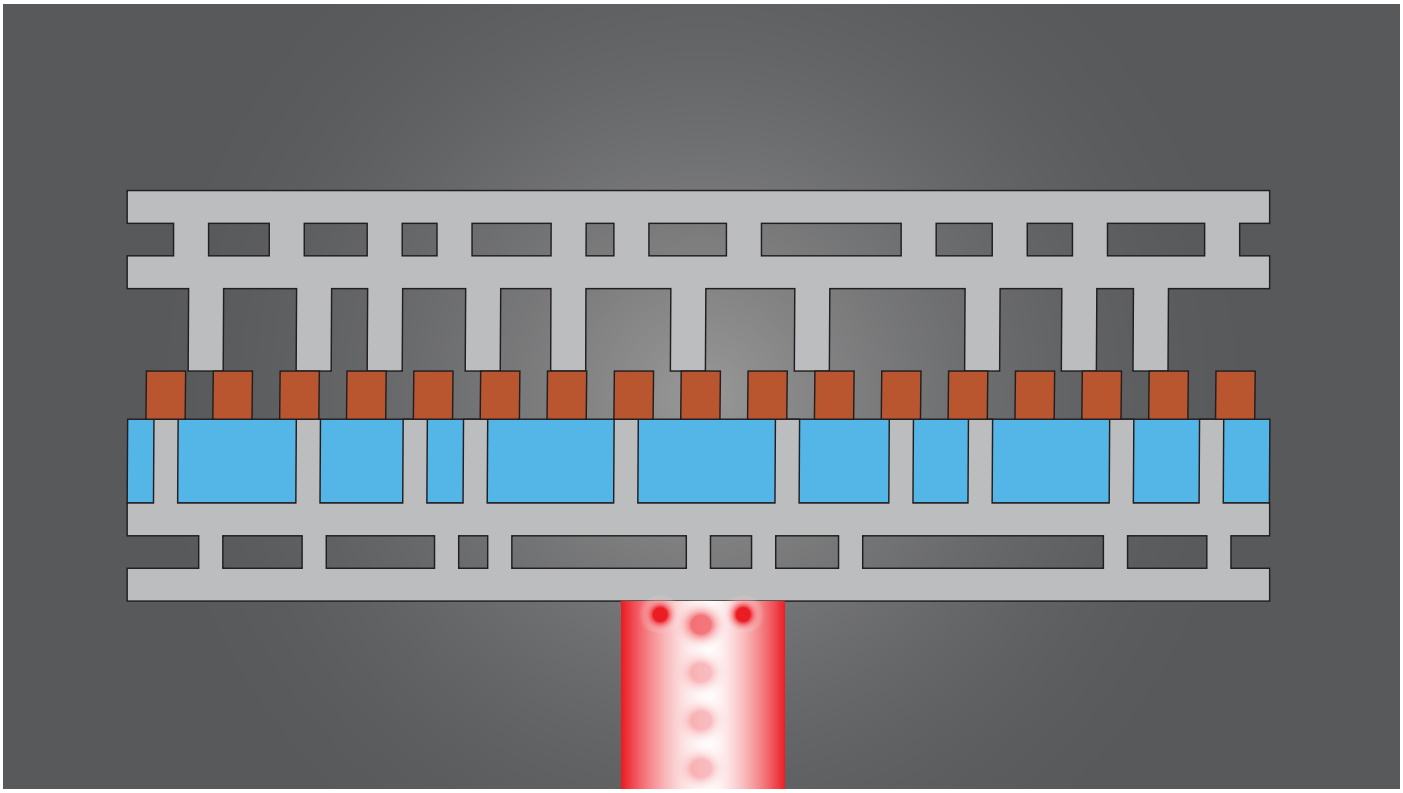

Figure 1. Optical (laser) fault isolation (OFI) is typically performed from the back side of the device, as the laser beam can pass through the silicon to interact with the gate structures. The introduction of back side power delivery networks causes the laser light to be blocked, effectively making backside access to the transistors impossible without some form of prior FIB preparation.

E-beam probing is now a "must-have" for FA

The reduction in feature size, GAA 3D complexity, and the adoption of backside metal layers for power distribution (BPDN) have not only increased the number of failures which need to be analyzed, but also require new FA processes to perform effective, high-success-rate root cause analysis. Many of these challenges are outlined in the EDFAS FA roadmap [1]. These FA processes typically encompass fault isolation, sample prep (delayering), transistor probing, sample preparation, and, finally, the production of imaging and elemental data from a TEM (transmission electron microscope).

For coarse localization, engineers can still use existing optical fault isolation (OFI) techniques, which can localize defects down to the hundreds of nanometers. The feature sizes seen with FinFET and GAA structures now additionally require a significantly finer resolution to narrow defect location to a few transistors or tens of nanometers; this requires electron beam (e-beam) probing. Compared to OFI, e-beam probing provides a 10× improvement in resolution, thus playing an essential role in GAA failure analysis [2,3,4].

In addition to its SEM voltage contrast capability, which can diagnose and localize defects that may be buried within very complex wiring or power distribution networks, e-beam probing is also used to perform electron voltage imaging (EVI), electron voltage probing (EVP), and e-beam-induced resistance change (EBIRCh) applications that can localize electrical defects while the device is powered up and connected to an external test system as shown in Figure 3 (following page).

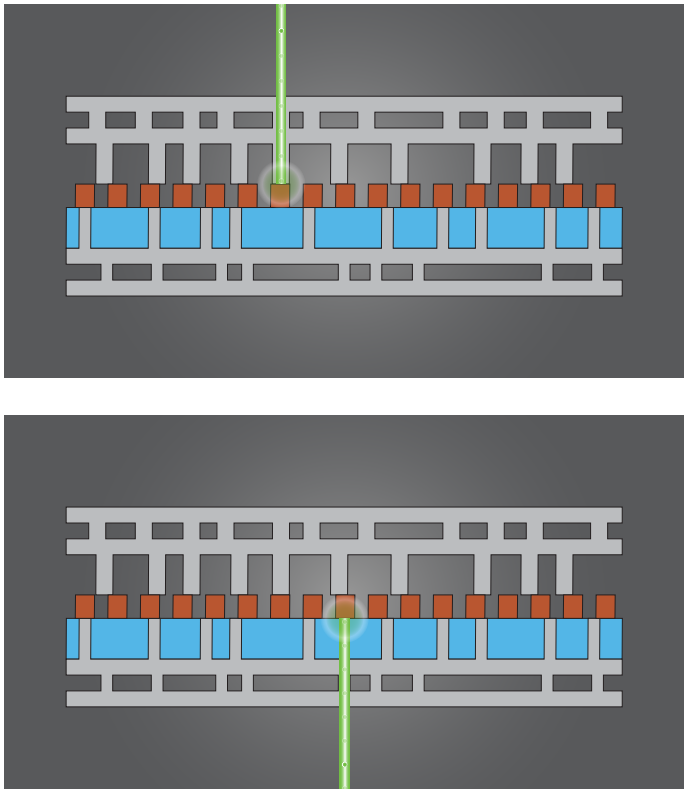

Figure 2. E-beam fault isolation (EFI) can be performed from the front or the back side of the device, as the e-beam can pass through the metal interconnects to reach the active area. EFI also offers significant resolution advantages versus optical techniques.

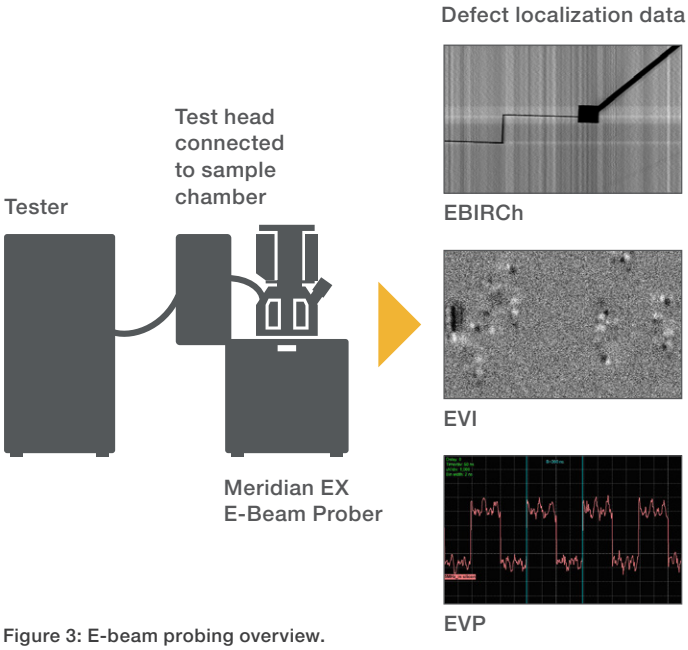

Figure 3: E-beam probing overview.

High-performance DualBeam FIB-SEM systems and their fundamental importance to logic FA

Backside power distribution has introduced additional challenges to failure analysis workflows. First, the power distribution wiring itself may contain defects, and these are generally localized using thermal (Thermo Scientific™ ELITE™ System) or optical (OFI) techniques. For fault localization within structures and active areas buried beneath the power distribution network, new workflows are required to gain access using precise delayering from either the front side or back side of the die. This can be accomplished with conventional DualBeam™ plasma FIB-SEMs (focused ion beam scanning electron microscopes). In recent years, new platforms have been developed with FIB technology that can provide the high success rate, precise end pointing, sample quality, and productivity required by leading FA labs. Recent innovations targeted at advanced logic FA applications include:

- High-quality, high speed, cross-section milling with high-power, focused Ar^+ FIB-SEM.
- Delayering with Xe^+ PFIB-SEM prior to nanoprobing or e-beam probing.
- Low-beam-current, highly automated Ga^+ FIB for high-quality TEM sample preparation.

It's not an overstatement to say that most FA applications now require some form of focused ion beam (FIB) preparation, and high-performance FIB-SEM instruments are now core elements of advanced logic failure analysis workflows. As shown in **Figure 4**, a typical workflow including several key FIB-SEM steps such as cross-section SEM imaging of packaging failures, preparation for OFI, EFI, and nanoprobing, and, finally, high-quality TEM sample preparation at the exact defect location.

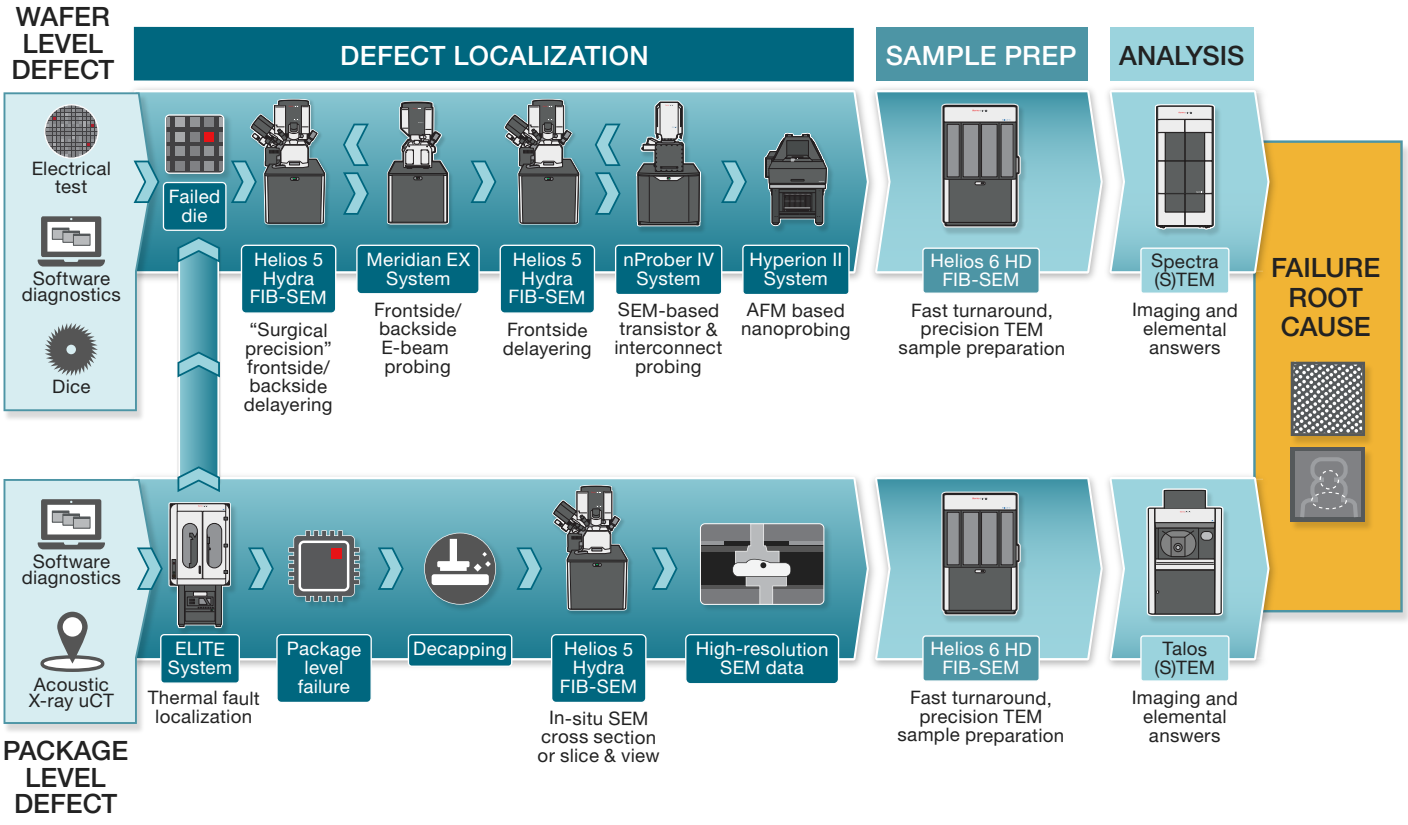

Figure 4. Typical FA workflow for advanced logic devices.

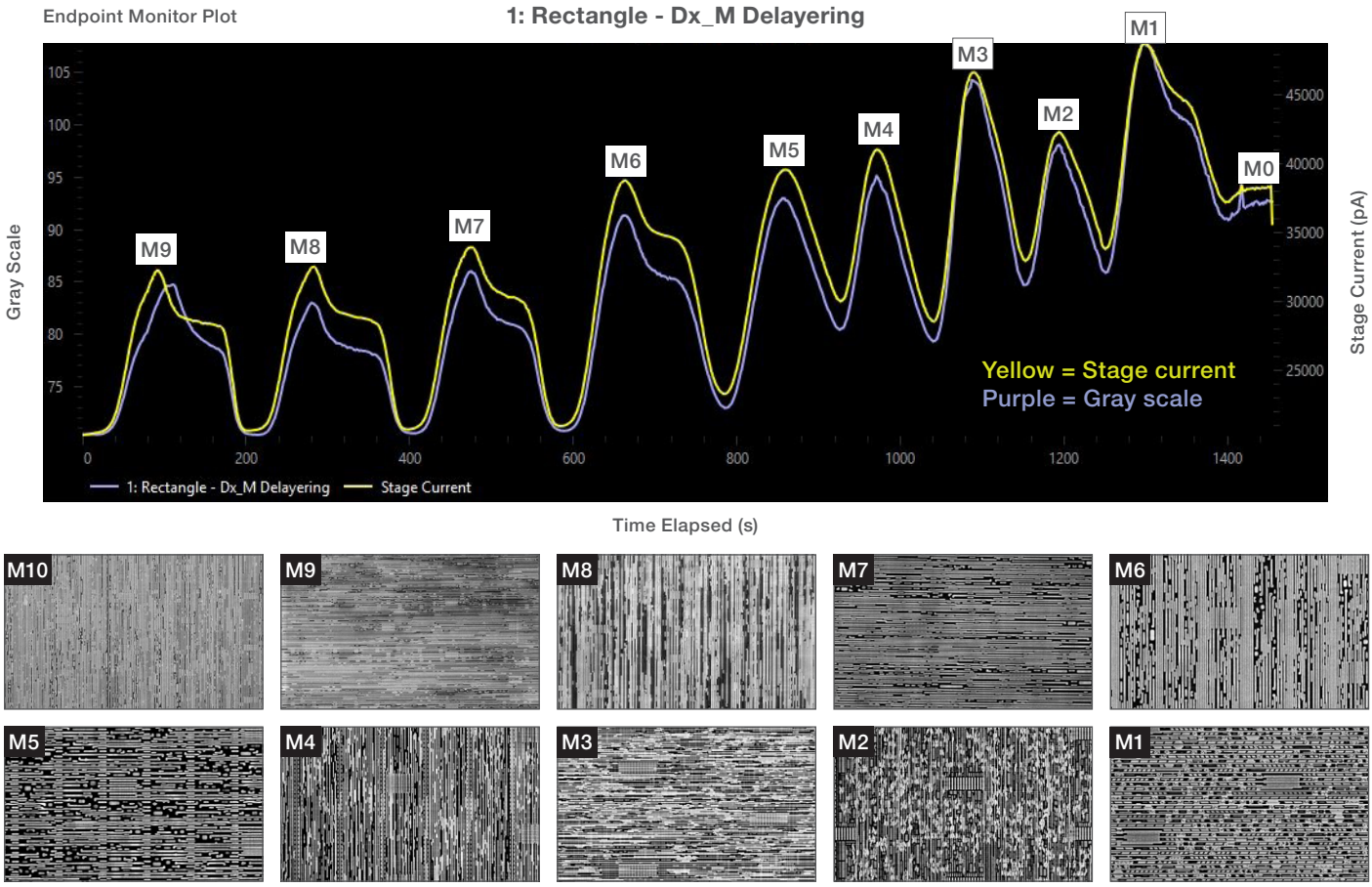

Figure 5. Delayering a 5 nm device from M10 to contact layer using the Helios Xe⁺ FIB. Also shown is the stage current graph, used for end-pointing on each layer [5].

Nanoprobing workflows have also evolved to meet GAA challenges

Once the defect has been localized accurately, additional probing is often required to confirm the electrical performance of individual transistors within a functional circuit. Nanoprobing enables FA engineers to identify and characterize which transistor or interconnect has actually failed. Accurate identification of a defect location sets the stage for the subsequent STEM analysis that provides the ground truth data for root cause failure diagnosis. Nanoprobing has been used for many years to characterize and isolate electrical defects that can negatively influence yield, reliability, and performance. Its ability to localize with such precision and accuracy is now critically important in ensuring the success rate of any subsequent STEM analysis.

In its simplest form, nanoprobing is accomplished by performing Xe⁺ FIB delayering to the desired layer, then precisely positioning nanoprobes onto the circuit, which are in turn connected to an electrical test system that can check continuity, transistor I/V curves, etc. Nanoprobing at the most advanced nodes now requires dedicated, standalone instruments that can provide the automation, stability, and accuracy required to land probes on the contact layer. Nanoprobing at these nodes also requires an automated Xe⁺ PFIB instrument that can accurately end-point on the correct layer without altering the underlying transistor performance [5].

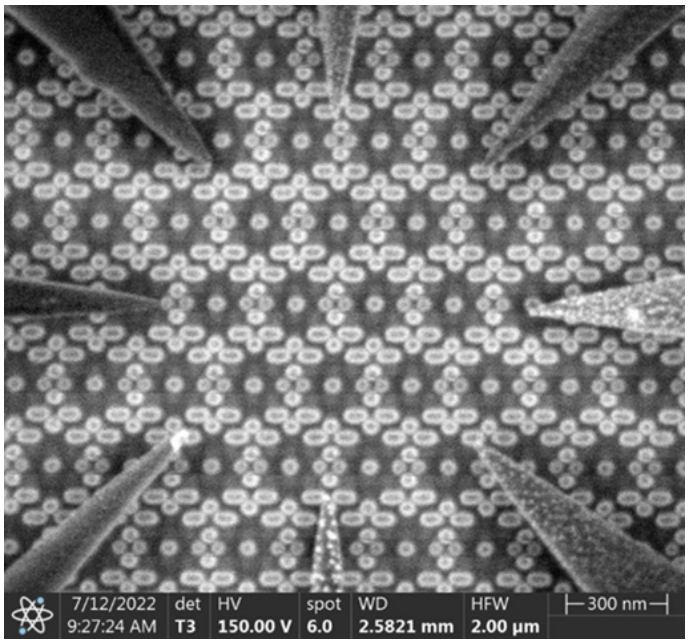

Figure 6. Nanoprobing a 5 nm device.

Recent nanoprobing innovations have evolved to specifically meet advanced logic challenges. One example is the ability to probe individual source-drain channels within a GAA transistor by preparing a sample in a FIB-SEM and probing it while attached to a TEM grid. Another is the use of Xe⁺ PFIB milling to create an isolation trench, which enables probing of a logic cell without interference from surrounding circuitry[6].

Once you have found the defect, now what?

The next step is usually physical failure analysis (PFA) in a TEM. This involves the creation of a high-quality TEM sample, which may be only a few tens of nanometers in thickness and must perfectly capture the region of interest while removing any obscuring or obfuscation by structures surrounding the defect. Once an artisan and very manual process, TEM sample preparation at the sub-5 nm node is now a routine process, largely due to the use of automated routines for repetitive functions such as alignments, calibrations, and sample manipulation to ensure highly repeatable results. But the technology continues to evolve to serve the needs of the FA roadmap. The use of AI automation and low-kV FIB performance are both playing an increasingly important role in making this TEM sample process more productive and more repeatable.

The sample can then be transferred to a TEM for the acquisition of high-quality, atomic-level imaging and elemental data. A lot of investment has been made into the sample once it reaches this final step. Obviously, damaging these valuable samples must be avoided. The days of TEM scientists spending hours on a sample to extract the data required are long gone. TEM must now deliver answers quickly, in the order of 5–10 samples per hour. These answers may include atomic-level imaging, high-resolution elemental analysis, and trusted, repeatable metrology data. And all of this must also be done while minimizing the electron dose, which must be carefully managed to avoid damaging the sample or reducing the quality of the final data. Again, the use of automated alignments and auto-functions is key, as well as high-speed acquisition of the desired data. TEM is now relied upon to provide the ground truth answers in most logic FA cases.

Summary

Failure analysis on advanced logic devices is often described as finding a needle buried deep within a haystack. Failure analysis engineers must determine the physical root cause of a failing device despite the increases in structural and materials complexity as well as the sheer number of transistors per device. Finding subtle physical and electrical defects requires continuous innovation in the areas of e-beam probing, FIB technology, and TEM workflows. Fortunately, due to machine learning-based automation and continued hardware innovations, the crucial metrics of time to data and success rate continue to be met.

To learn more about Thermo Fisher Scientific's semiconductor solutions that support advanced logic development and manufacturing, please visit:

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Acknowledgments

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List of Abbreviations

AI – Artificial intelligence

BPDN - Buried power distribution network

EFA - Electrical fault analysis

EFI - Electrical fault isolation

EVI - Electron voltage imaging

EVP - Electron voltage probing

EBIRCH - E-beam induced resistance change

FA – Failure analysis

FIB - Focused ion beam

FIB-SEM – Focused ion beam and scanning electron microscope

GAA – Gate-all-around

IDM - Integrated device manufacturer

OFI – Optical fault isolation

PFA - Physical failure analysis

PFIB-SEM - Plasma focused ion beam and scanning electron microscope

SEM - Scanning electron microscope

STEM – Scanning transmission electron microscopy

TEM – Transmission electron microscopy

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