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Effect of Parasitic Capacitance on ESD Simulators

A review of the effects of parasitic capacitance on HBM waveforms

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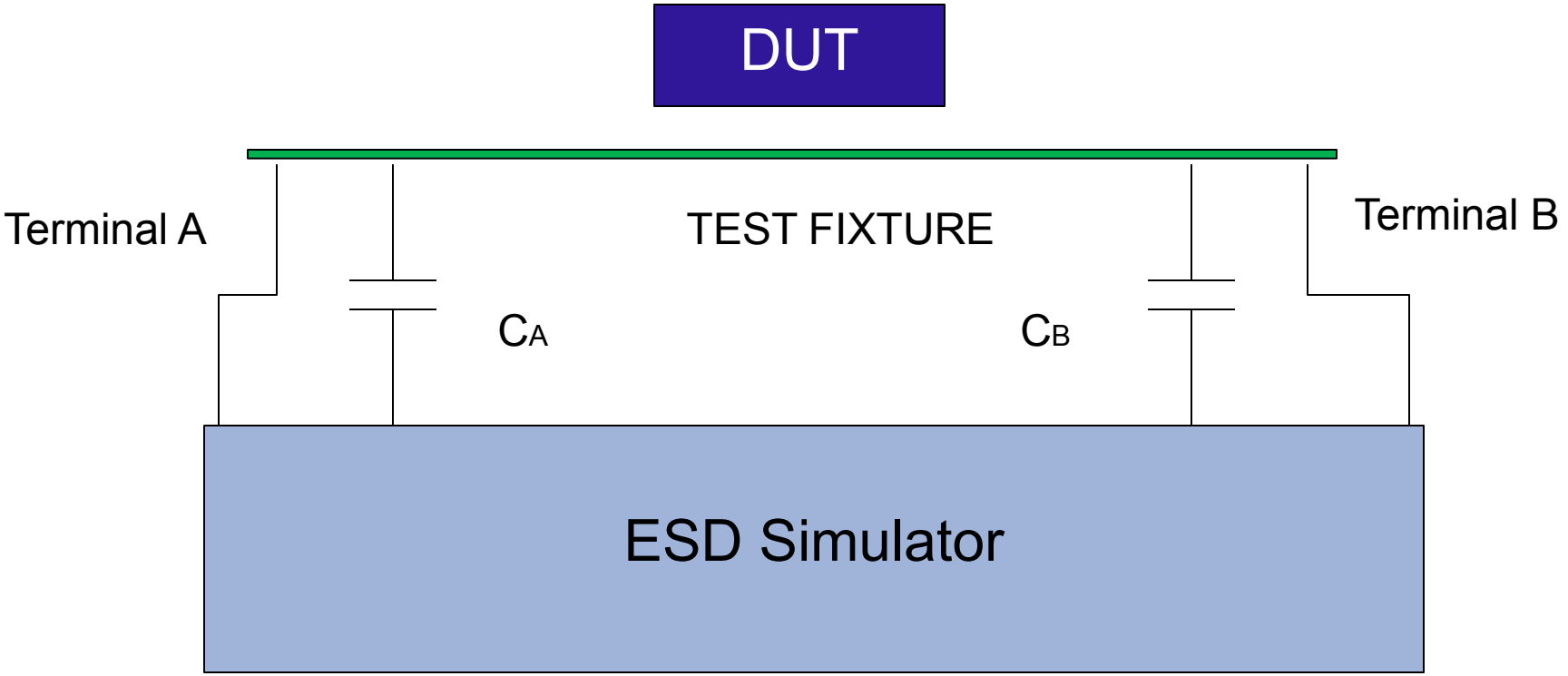
Parasitic capacitance on ESD simulators

- High pin count ESD simulators rely on relays to be able to switch connections that allow the simulator to perform multifunction operations on the DUT
- Relays, wiring and traces contribute with both parasitic inductance and capacitance.
- Parasitic capacitance plays an important role when multiple pins are tied together because their parasitic capacitance adds up, potentially changing the simulated ESD waveform

Objectives

- Gathering data for many different of DUT should involve pins tied together in terminal A, terminal B or both.
- Construct an accurate SPICE model: Model should replicate an accurate real HBM waveform using a two terminal model and reflect values of real construction components
- Determine the effects of added capacitance to terminal A
- Determine the effects of added capacitance to terminal B
- Determine the effects of added capacitance to terminal A and terminal B
- Determine what possible effects each of of this cases could have on device testing.

ESD simulator model block diagram



SPICE simulation

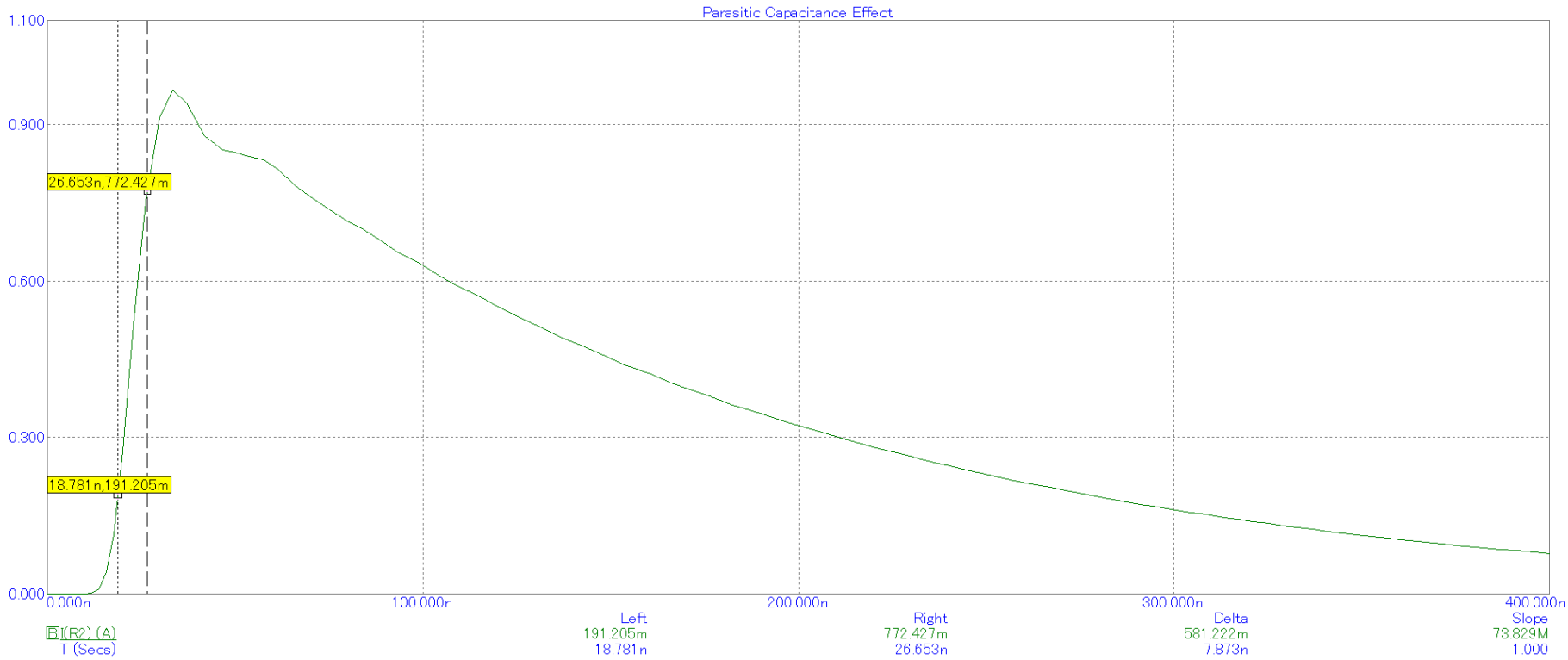


Figure 1.Base waveform Tr = 7.9ns

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C_A from 5-200pF

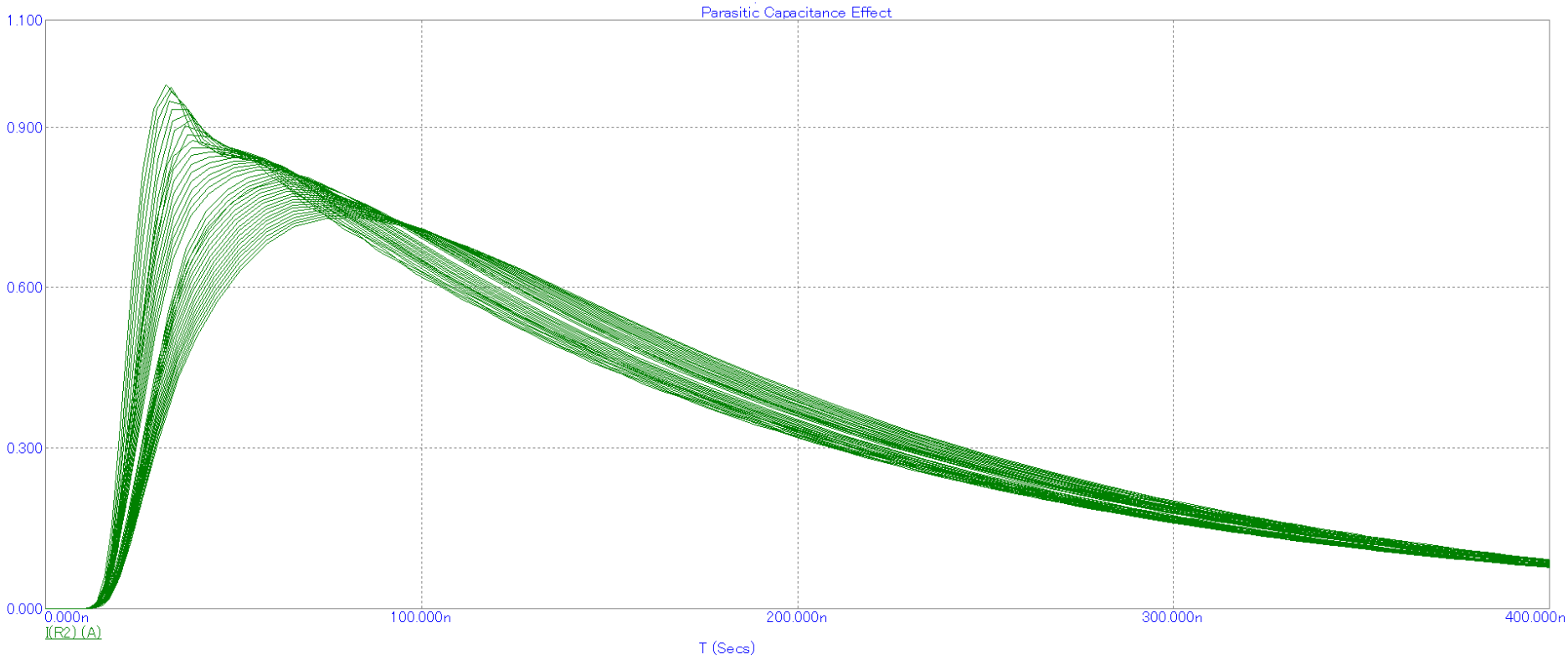

Figure 2. Simulation of parasitic capacitance on Terminal A

SPICE Results for varying C_A

C_A (pF)	Rise Time (ns)	Peak Current (A/1500v)
20	8.41	0.949
40	10.53	0.902
60	13.19	0.853
80	17.31	0.834
100	23.6	0.817
120	30.19	0.799
140	38.18	0.779

Table 1. Simulation of parasitic capacitance on Terminal A

Trend on Rise Time and Amplitude when Varying C_A

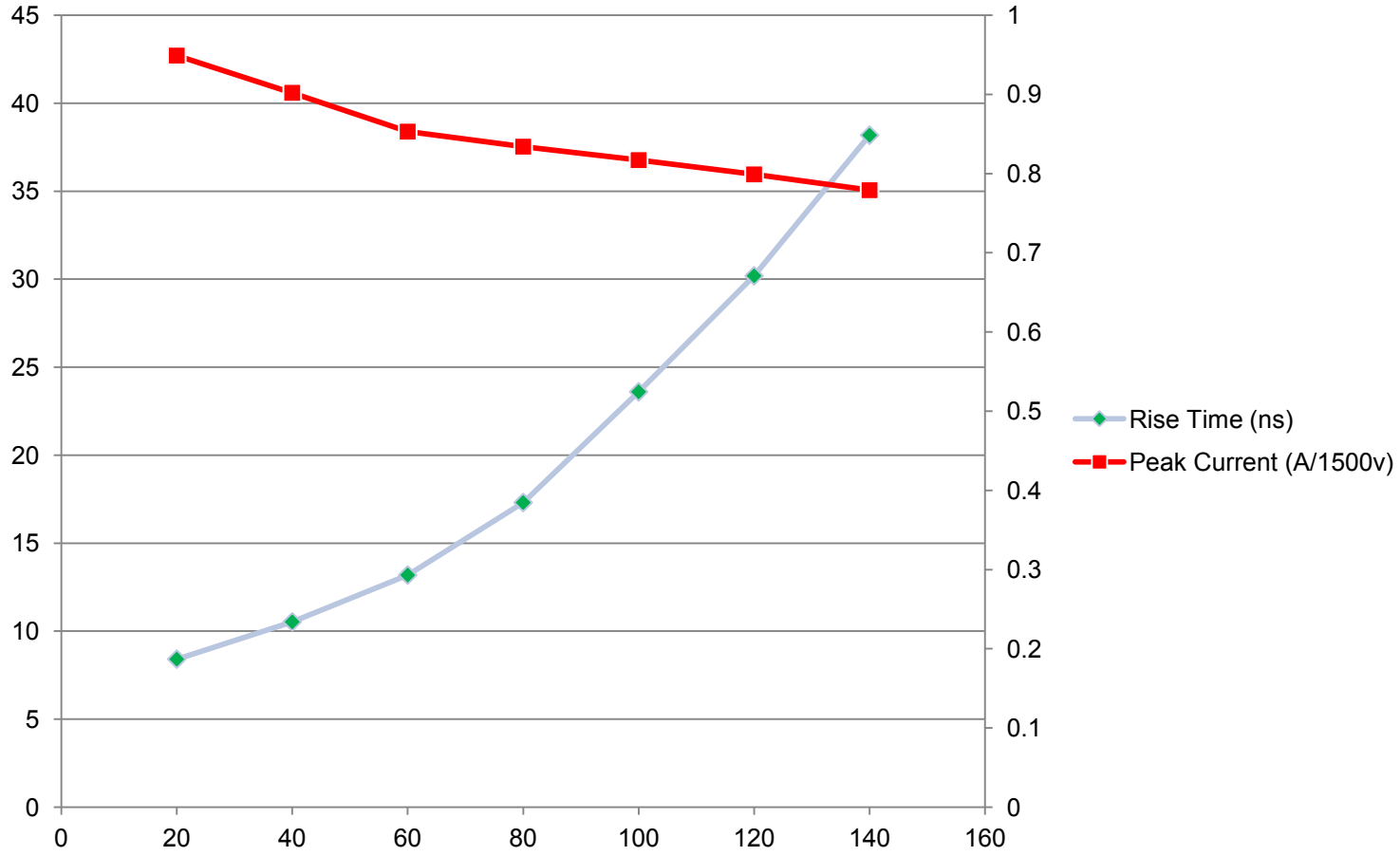

Figure 3. Simulation of parasitic capacitance on Terminal A

SPICE simulation results for varying values of C_A and C_B

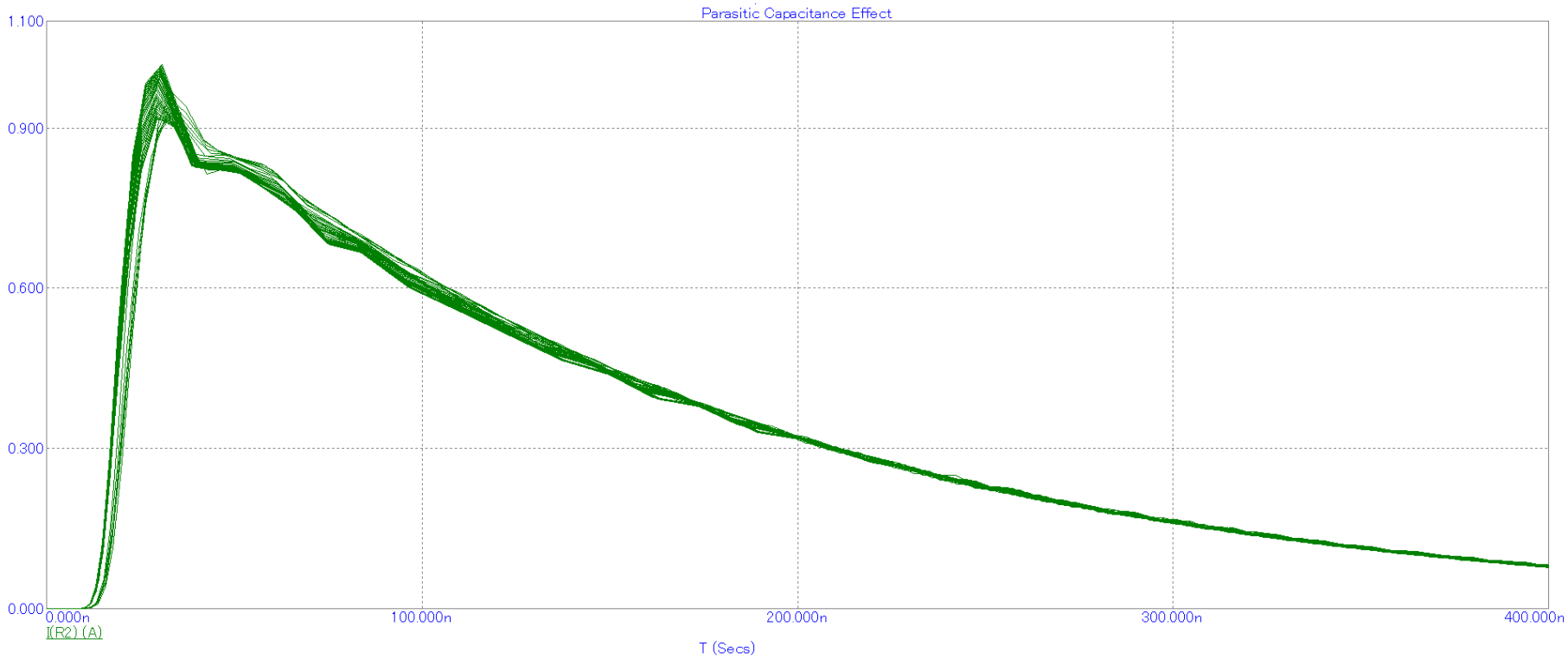

Figure 4. SPICE Simulation of parasitic capacitance on Terminal B

Table results for Rise Time and Amplitude for varying C_A and C_B

C_B (pF)	Rise Time (ns)	Peak Current (A/1500v)
20	8.61	0.936
40	8.29	0.919
60	7.74	0.934
80	7.26	0.951
100	6.85	0.961
120	6.52	0.981
140	6.44	0.993

Table 2. Simulation of parasitic capacitance on Terminal B

Trend of values of Rise Time and Amplitude when varying C_A and C_B

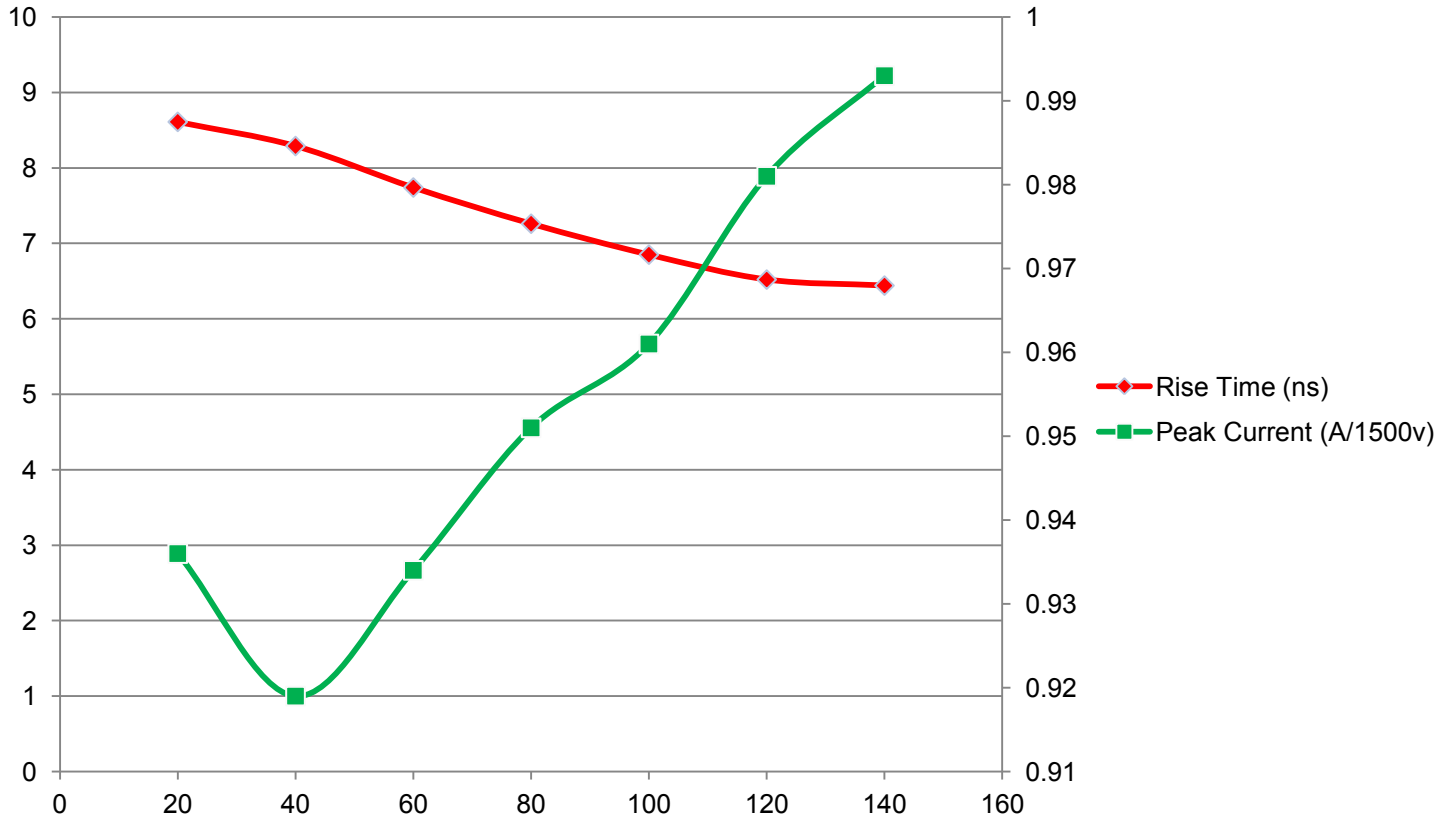

Figure 5. SPICE Simulation of parasitic capacitance on Terminal B

Table of Results for Rise Time when Varying C_A and C_B

C_A (pF)	C_B(pF)	Rise Time (ns)	Peak Current (A/1500v)
20	20	8.27	0.920
40	40	8.5	0.832
60	60	9.00	0.799
80	80	8.86	0.766
100	100	8.84	0.740
120	120	8.67	0.716
140	140	8.4	0.694

Table 3. Simulation of parasitic capacitance on Terminal A and B

Trend of Rise Time and Amplitude with Varying C_A and C_B

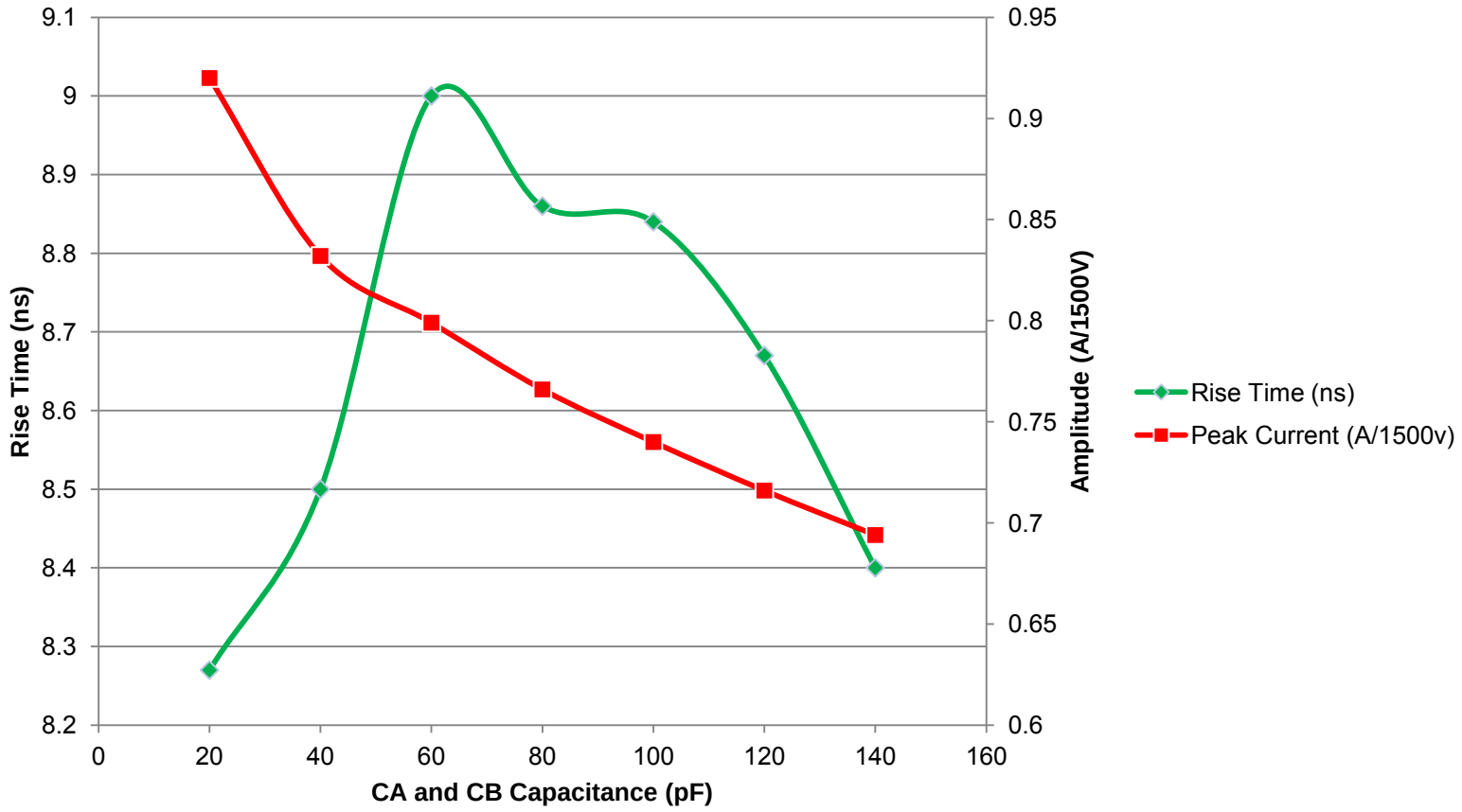

Figure 6. SPICE Simulation of parasitic capacitance on Terminal A and B

What does all of this mean?

- Three general cases
  - Multiple pins on terminal A
  - Multiple pins on terminal B
  - Multiple pins on both terminal A and terminal B
- Devices with multiple pins on terminal A have lower than normal amplitudes and slower rise times. If protection structure is rise time sensitive, the slower rise times might cause the protection structure to fail. If the protection structure is amplitude sensitive, the protection structure might fail.
- Devices with multiple pins on terminal B will cause faster rise times and possibly higher than normal amplitudes. These two can also cause protection structures to fail due to one or the other.
- Devices with multiple pins on both terminal A and terminal B remain with a relatively constant rise time but lower amplitudes.

Effects of parasitic effects on device testing

- Parasitic capacitance might cause a device to fail at:
  - A lower test voltage
  - A higher test voltage
  - No change in testing
- It all depends on the design of the ESD protection structure

Multiple pins Vs two pin testing

- In the real world a device with many pins is more likely to suffer a discharge involving multiple pins, rather than selectively only two pins, making parasitic part of real world testing.
- Low pin devices, on the other hand, have better chances of being exposed to a lower pin count ESD stress, making two pin test better suited for low pin count devices.
- Any time there is a test in question while testing on a relay based high pin simulator, a two pin simulator should be considered, but careful engineering consideration should be exercised to determine if the effect of parasitic capacitance is truly causing a false failure and not simple as a tool to make the DUT test better. The ultimate goal is to have a more reliable device.

Limitation of the simulation

- SPICE simulation is based on a careful study of a real HBM ESD simulator, but errors in simulation are still possible. The data should also be investigated with long term devices.
- Complex interaction between DUT and simulator are not considered, in this simulation the DUT is considered to be purely resistive.
- Complex interaction between the DUT and the simulator could alter the data presented significantly.
- Simulators with low impedances and low losses such as a 50 Ohm system or a TLP system could cause interactions such as reflections that will normally not be present in higher impedance systems.

Conclusions

- Two pin ESD simulators offer a new tool in testing for ESD susceptibility
- Engineering judgment should be exercised to determine if an unexpected failure is due to parasitic capacitance, a flaw in protection structure design or a process problem.
- Two pin testing could render results that are better that multi-pin system, worse or the same