



- What are parasitics and their associated effects?
- > What causes parasitics?
- Do parasitics actually affect my testing?
- What can I do to reduce these effects?
- How has Thermo Fisher Scientific solved this problem?
- Correlation testing results.
- ➢ Introduction to the Thermo Scientific™ Ultra Low Parasitic (ULP) MK series tester.



What are parasitics and their associated effects?

- Parasitics, or better stated, parasitic capacitance or stray capacitance, is an unavoidable and usually unwanted capacitance that exists between parts of an electronic component or circuit, simply because of their proximity to each other and or ground.
- Since HBM simulators are designed to have a tight geometry, in order to control the integrity of the waveform, parasitics have always been part of the equation, even though the Simplified HBM Tester Model doesn't take them into account.





What are parasitics and their associated effects?

- However, automated testing is generally not a perfect world, as the need for speed and repeatable testing makes it impossible, or at least it use to, to make a tester that isn't affected by parasitics.
 - The parasitics haven't always affected device test results but as geometries shrank and technologies evolved, parasitics began to effect these newer devices, although some times showing weaknesses in protection structure designs!
- Parasitic capacitance effects circuits, in this case our HBM circuit by either limiting the amount of energy that can be forced onto a pin or by adding to the energy, as the parasitic elements store charge then release it at the time of the intended event, causing a higher energy waveform than expected.
 - In either case, parasitics can play a role in the eventual determination of the failure threshold level of your devices, as the device itself influences how the parasitic capacitance elements will react – different protection designs protection different impedances all play a role!
 - Rise time triggered protection structures may be more susceptible than others, as the reduction in the rise time caused by the parasitics can cause the protection structure to react slowly, or even worse not at all!

What causes parasitics?

> In an HBM simulator there are a number of parasitic elements



- Test fixture boards have capacitance between etch runs and system ground. Higher pin count, multilayer boards increase these parasitics.
- > DUT sockets have capacitance between contacts and the socket body
 - The test fixture board and DUT socket combination are generally referred to as variable parasitic elements, as no two DUT fixture boards are designed the same, although our design criteria helps minimize this.
- Pogo pins and their associated relays have a capacitive element to other components on the matrix, as well as system ground.
 - The relay matrix and pogo pins are considered to be fixed parametric elements as they stay relatively constant. These play the biggest role in system parasitics!



What causes parasitics?

- An schematic overview of some of the parasitic elements in testers ^[1]
 - Pin to pin in the socket
 - Trace to trace on the fixture
 - Pogo pin to pogo pin
 - Relay to relay on the matrix
- The 1998 paper on the "Investigation into SDM Tester Parasitics" ^[1] was the first to outline in detail, where these parasitic elements are located.
- M. Chaine, et al., "Investigation Into Socketed CDM (SDM) Tester Parasitics," EOS/ESD Symposium Proceedings, 1998, pp. 301-310.





- What a question!! And, depending on who you ask, you'll get different answers based on their companies protection design philosophy.
- There have a been a number of papers on the effects of parasitics on device testing, starting as early as 1993^[2]. This paper was the first to highlight the need for control of the fixture capacitance and introduced the 500Ω measurement to the standards.
 - The schematic below shows the HBM circuit, including the newly added board capacitance element, C₂



Fig. 3. The LEM HBM circuit [5], containing the HBM elements C_{hb} and R_{hb} , a shunt capacitance C_1 across R_{hb} , the test board capacitance C_2 and the series inductance L_1 of the discharge path. R_1 stands for the load resistor.

[2] K. Verhaege, et al., "Analysis of HBM Testers and Specifications using a 4th Order Lumped Element Model," in Proc of EOS/ESD Symposium, 1993, pp 129-137.



- A paper in 2004 highlighted the effects that the parasitics played when testing using the standard zap combinations, using both polarities^[3].
 - The subject device reacted differently when stressed negatively from IO to Vdd. This was due to the fact that their protection structure design summed the capacitance of other "floating" IO pins on the device, causing a much lower than expected failure threshold.



Figure 11: Possible Current Paths to Charge Tester Relay Capacitance- IO Negative With Respect to VDD.

Their work around was to eliminate the negative stress from IO to Vdd and perform a positive Vdd to IO.

[3] H. Kunz, et al., "The Effect of High Pin-Count ESD Tester Parasitics on Transiently Triggered ESD Clamps", 2004 EOS/ESD Symposium Proceedings.



- \succ In 2006, a paper by M. Chaine, et al., ^[4] discussed the effects of the so called "floating pins" had on device test results during HBM testing on a high pin count tester.
- \succ The diagrams below from the paper, show how the current flowing through Terminal B is affected, as the parasitics of the additional "floating pins" are connected in parallel with the return path of the HBM pulse.



Figure 7 schematic illustrates the case when "n" pins are connected in parallel

L2s

R₂s

[4] M. Chaine et.al., "HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins", EOS/ESD 2006 Proceedings, pg. 06-354



- As a follow-up to their 2004 paper, TI presented another paper in 2010 highlighting the use of 2 pin testing and TLP testing to verify their original findings^[5].
 - This paper also discussed suggested changes to the JEDEC standard^[6] to allow alternative zap combinations(Vdd to IO) and allow device qualification across multiple testers.
- So, after these long answers, the simple answer is yes, parasitics can affect test results.
 - The caveat to this is that some suspect results, may be pointing to issues with protection designs

[5] S. Ward, et al., "Overcoming the Unselected Pin Relay Capacitance HBM Tester Artifact with Two Pin HBM Testing", 2010 EOS/ESD Symposium Proceedings [6] JEDEC Standard, JESD22-A114-F, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).



What can I do to reduce these effects?

- In our White Paper from 2007^[7] we discussed the use of templates to isolate the untested pogo pins from the test fixture as a way to truly float the unselected pins
- Alternative pin combinations, such as TI's approach to their IO to Vdd issue – stress Vdd to IO with a positive pulse only can be used
- Two pin testing can be performed on suspect pins after performing a complete test on your relay based tester
 - The Joint Standard, JS-001 provides new guidelines for pin combinations to help minimize the parasitic effects but still suggest the part be fully tested on an automated tester and if questionable results arise, use alternate combinations or two pin testing methods
 - Two pin testing methods range from using a two pin tester, such as our Pegasus system to isolating unused pins on your automated tester
 - Pegasus presentation to follow

[7] R. Given, T. Meuse, I. Morgan, "Study of the Impact of Non-selected I/O Pins During HBM Test Using ZapMaster MK.2", Conformity September 2007



What can I do to reduce these effects?

- ➤ Another option, use a matrix based Ultra Low Parasitic (ULP) tester, like the Thermo Scientific[™] MK.2-ULP system!
 - Last year we presented a paper at the RCJ symposium in Japan^[8] which highlighted the work we've done on minimizing parasitics on the MK2 tester.
 - We also presented visitors at the 2012 EOS/ESD symposium with a copy of the paper and a presentation^[9] outlining our progress on this exciting new break-through!

[8] M. Hernandez, et al., "Parasitic Capacitance Effects on HBM ESD Simulators and Device Testing", 2012 RCJ Symposium, pp 83 – 89, 22E-09 [9] Thermo Fisher Scientific, "Low parasitic in high pin count tester", 2012 EOS/ESD Symposium, provided in a handout format



How has Thermo Fisher Scientific solved this problem?

- To fully understand the impact of the parasitic capacitance elements and their interaction with device under test, we created an detailed SPICE model, taking into account many variables to help create an accurate simulation of an HBM waveform using a two terminal model
- Simulations were done to determine the effects of added capacitance in 3 different combinations of loading:
 - Terminal A only
 - Terminal B only
 - Both terminal A and terminal B



Simulations followed the trend that has been reported in previous papers, armed with this information we were able to review the system design and make advanced improvements in the architecture





How has Thermo Fisher Scientific solved this problem?



SPICE simulation of a 1500V HBM waveform as the parasitic capacitance on C_A is increased from 5pF to 140pF

Graph of amplitude and rise time vs. parasitic capacitance at terminal A



How has Thermo Fisher Scientific solved this problem?

- SPICE Modeling provided us with insight to changes required in the system architecture to minimize the parasitics on each system channel.
 - With changes implemented on a system, waveforms could be evaluated and compared against the SPICE model. By adding connections to additional floating pins on the tester, through the use of Shorting Modules like those called out in the joint JS-001-2012 standard^[10] we were able to verify the system changes followed the SPICE modeling.
- Using the SPICE model calculations and through measurement of the new hardware, we determined that the new architecture reduced parasitic capacitance by approximately a factor of 10 on each system channel, with an overall factor of 5 across the complete system.

[10] ANSI/ESDA/JEDEC JS-001-2012



- Before performing actual device correlation testing, verification of the waveform performance against the JS-001-2012 "Test to Determine if an HBM Simulator is a Low-Parasitic Simulator" had to be performed.
 - > JS-001-2012 definition of a Low Parasitic HBM Simulator
 - A Low Parasitic HBM simulator will have nearly identical currents on Terminal A and Terminal B when testing a pair of pins of a multi-pin device.
 - A shorting module, similar to the one shown in Figure 10 of the standard was used.



Figure 10: Diagram of a 10-pin Shorting Test Device Showing Current Probe





HBM waveform on a standard MK2, when ten pins are tied together at terminal B





HBM waveform of a reduced parasitics ESD simulator (Thermo Scientific MK2-ULP), when ten pins are tied together at terminal B

Device Correlation Testing

	Standard MK2	MK2-ULP
Device A	5kV failure, correlating to previous data	No failures on 5 devices tested to 8kV
Device B	Failure level unknown	6 devices tested at +1kV, no failures 6 devices tested at -1kV, no failures Indication from the manufacturer was they expected to see failures at this level if parasitics were present

